

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1. (currently amended) A switching mode power supply comprising:  
a rectifier configured to convert AC power to a first DC power;  
an output unit configured to convert the first DC power to a second DC power  
under the control of a first switch; and  
a pulse width modulation generator coupled to control the first switch, the pulse  
width modulation generator having a regulator configured to regulate the first DC power, the  
regulated first DC power powering the pulse width modulation generator, the regulator  
comprising a second switch coupled to control a transmitter so that when the second switch is in  
a first state the transmitter transmits the first DC power to a capacitor to charge the capacitor to  
thereby increase the regulated first DC power, and when the switch is in a second state the  
transmitter does not transmit the first DC power to the capacitor to thereby allow the charge in  
the capacitor to reduce and the regulated first DC power to decrease.
2. (original) The switching mode power supply of claim 1 wherein the  
regulator further comprises a power supply voltage manager configured to bias the second switch  
so that during normal mode of operation the regulated first DC power is maintained at a  
substantially constant voltage level.
3. (original) The switching mode power supply of claim 2 wherein the  
regulator further comprises a switch core coupled between the power supply voltage manager  
and the second switch so that during a power up mode the switch core biases the second switch  
in the first state until the regulated first DC power reaches a predetermined power level, and  
during the normal mode of operation the switch core couples an output of the power supply  
voltage manager to the second switch.

4. (original) The switching mode power supply of claim 2 wherein the power supply voltage manager comprises a comparator configured to compare a first voltage derived from the regulated first DC power to a reference voltage and in response output a signal for biasing the second switch such that the regulated first DC power is maintained at the substantially constant voltage.

5. (original) The switching mode power supply of claim 2 wherein the regulator is a switched-mode regulator.

56. (currently amended) An SMPS (switching mode power supply) comprising:

a power supply for converting AC power to DC power and outputting the DC power;

an output unit including a transformer having a primary coil[[],] one end of which is coupled to the power supply, ~~for the output unit~~ outputting the power transmitted to a secondary coil of the transformer from the power supply;

a switching driver including a first switch coupled to another end of the primary coil of the transformer, and a first capacitor coupled to store power derived from the DC power, the power stored in the first capacitor powering the switching driver, the switching driver for generating a second power according to the first power applied by the power supply, for generating a PWM (pulse width modulation) signal[[s]] according to the second power to drive for driving the first switch; and

a feedback circuit for feeding back to the switching driver an output signal provided power output by the output unit to the switching driver,

wherein the switching driver comprises:

a high-voltage regulator for supplying the ~~first DC~~ power to the first capacitor when the level of the ~~second~~ power ~~charged stored~~ in the first capacitor is less than a first level, and preventing intercepting the first DC power applied from being supplied to the first capacitor when the level of the second power stored in the first capacitor is greater than a second level;

a PWM generation unit for generating the PWM signals and supplying them to the first switch; and

a UVLO (under-voltage lockout)/bandgap unit for starting operation when the second power in the first capacitor reaches a predetermined level, and controlling the operation of the PWM generation unit.

67. (currently amended) The SMPS of claim 56, wherein the high-voltage regulator comprises:

a JFET coupled to the power supply for lowering the level of the DC power; and a second switch for forming or intercepting controlling a current path between the JFET and the second first capacitor in response to an enable signal from generated by the UVLO/bandgap unit.

78. (currently amended) The SMPS of claim 56, further comprising: an oscillator for generating a clock signals by under the control of the UVLO/bandgap unit, and supplying the clock signal to the PWM generation unit; and a comparator for comparing a the feedback signal voltage supplied by the feedback circuit with the clock signal outputs of the oscillator, wherein the PWM generation unit controls the duty ratio of the PWM signal[[s]] according to comparison results of the comparator.

89. (currently amended) The SMPS of claim 56, wherein the switching driver further comprises a protector for coupled to inhibit the PWM generation unit from generating a PWM signal starting operation when one of a number of predetermined events occurs the output voltage of the output unit is overloaded, and preventing generation of the PWM signals.

910. (currently amended) The SMPS of claim 89, wherein the switching driver further comprises a controller coupled to enable outputting an enable signal for a predetermined time when the voltage of the second power is greater than a threshold voltage, and the protector controls the PWM generation unit to generate the PWM signal[[s]] for the a predetermined period of time after the PWM generation unit is inhibited from generating a PWM signal due to

occurrence of one of the number of predetermined events in response to the enable signal from the controller.

1011. (currently amended) The SMPS of claim 56, wherein the power supply comprises:

    a full-wave bridge rectifier for receiving the AC power and rectifying the same; and

    a second capacitor for smoothing the power rectified by the full-wave bridge rectifier.

1112. (currently amended) The SMPS of claim 46, wherein the feedback circuit comprises:

    an amplifier for amplifying the ~~power~~ output signal provided by the output unit; a photo coupler coupled to conduct current in response to the for starting operation when the power amplified signal provided by the amplifier reaches a predetermined level; and

    a second capacitor coupled to the photo coupler such that the current conduction in the photo coupler impacts the charge stored in the second capacitor for charging the current supplied by the photo coupler to provide a feedback voltage.

1213. (currently amended) An SMPS (switching mode power supply) comprising:

    a transformer for receiving a DC power at one end of the a primary coil, and outputting power through the a secondary coil; and

    a switching driver including a transistor coupled between another end of the primary coil and a reference voltage, for generating a PWM (pulse width modulation) signal[[s]] for periodically turning on/off the transistor ~~to apply the PWM signals to a gate of the transistor,~~ and operating the transformer by the on/off operation[[s]] of the transistor,

    wherein the switching driver comprises:

a capacitor coupled to store power derived from the DC power, the power stored in the first capacitor powering the switching driver for being charged with a power supply voltage for generating the PWM signals;

a UVLO (under-voltage lockout)/bandgap unit for starting operation when the power in the capacitor supply voltage reaches a predetermined level;

a high-voltage regulator including: a switch for forming a path between configured to couple the power derived from the DC power the supply voltage and to the capacitor when the power supply voltage charged stored in the capacitor is less than a first level, and intercepting the path to decouple the power derived from the DC power from the capacitor when the power stored in the capacitor supply voltage is greater than a second level; and a switch core for controlling on/off operations of the switch according to an enable signal supplied by the UVLO/bandgap unit;

an oscillator for generating a clock signals according to operation by under the control of the UVLO/bandgap unit; and

a PWM generation unit for generating the a PWM signal[[s]] according to the clock signal[[s]].

1314. (currently amended) The SMPS of claim 1213, further comprising a feedback circuit for providing a feedback signal to the switching driver in response generating a feedback voltage according to an output signal provided by of the transformer, and supplying the feedback voltage to the switching driver, wherein

the PWM generation unit controls the duty ratio of the PWM signal[[s]] according to the feedback signal voltage.

1415. (currently amended) The SMPS of claim 1314, further comprising: a protector for coupled to inhibit the PWM generation unit from generating a PWM signal to thereby turning off the transistor when one of a number of predetermined events occurs the power supply voltage is overloaded or when the feedback voltage is an over voltage; and

a controller coupled to periodically enable the PWM generation unit to generate a PWM signal after the PWM generation is inhibited from generation of a PWM signal in order to determine whether the one of a number of predetermined events still persists for outputting an enable signal to the protector when the power supply voltage is greater than a threshold voltage during the operation of the protector, wherein the protector intermittently operates the PWM generation unit according to the enable signal from the controller.

1516. (currently amended) A PWM (pulse width modulation) signal generator including a transistor coupled between the a primary coil of the a transformer and a reference voltage, for supplying a PWM signal[[s]] to a gate of the transistor to periodically turn on/off the transistor and thus operate the transformer, comprising:

a high-voltage regulator including a JFET for receiving DC power and lowering coupled to lower a level of the a DC power;

a capacitor coupled to store power corresponding to the lowered DC power for being charged with the current supplied by the high-voltage regulator to form a power supply voltage;

a UVLO (under-voltage lockout)/bandgap unit for starting operation when the power supply voltage charged in the capacitor reaches a predetermined level;

an oscillator for generating a clock signal[[s]] according to under the control by of the UVLO/bandgap unit; and

a PWM generation unit for generating the PWM signal[[s]] according to the clock signals supplied by the oscillator, wherein

the high-voltage regulator supplies the lowered DC power to the capacitor when the level of the voltage charged power stored in the capacitor is less than a first level, and preventing intercepts the lowered DC power from being supplied to the capacitor when the level of the voltage charged power stored in the capacitor is greater than a second level.

1617. (currently amended) The SMPS PWM signal generator of claim 1516, wherein the high-voltage regulator further comprises:

a power supply voltage manager for regulating the power supply voltage charged ~~stored~~ in the capacitor;

a switch core for ~~receiving an enable signal generated by the UVLO/bandgap unit and transmitting a control signal from the power supply manager to a switch under the control of the UVLO/bandgap unit, the according to a voltage from the power supply voltage manager;~~

a switch being tuned on/off according to the control signal; and

a current transmitter for coupling the JFET to the capacitor when the switch is turned off, and ~~intercepting the coupling of decoupling the JFET to from the capacitor when the switch is turned off.~~

1718. (currently amended) The SMPS PWM signal generator of claim 1516, comprising:

a source/sink unit for receiving ~~a feedback signal derived from an output signal the voltage output by the transformer as a feedback voltage to determine a level of the feedback voltage;~~ and

a comparator for comparing an output of the source/sink unit with an output of the oscillator, wherein

the PWM generation unit controls the duty ratio of the PWM signal[[s]] according to a comparison result of the comparator.

1819. (currently amended) The SMPS PWM signal generator of claim 1718, further comprising:

a protector ~~for coupled to inhibit the PWM generation unit from generating a PWM signal to thereby turning off the transistor when one of a number of predetermined events occurs the power supply voltage is overloaded or when the feedback voltage is an over voltage;~~ and

a controller ~~coupled to periodically enable the PWM generation unit to generate a PWM signal after the PWM generation is inhibited from generation of a PWM signal in order to determine whether the one of a number of predetermined events still persists for outputting an~~

~~enable signal to the protector when the power supply voltage is greater than a threshold voltage during the operation of the protector, wherein~~  
~~the protector intermittently operates the PWM generation unit according to the enable signal from the controller.~~